LOW TEMPERATURE COEFFICIENT RESISTOR IN CMOS FLOW

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. Nonprovisional patent application Ser. No. 13/288,700, filed Nov. 3, 2011, and claims the priority of U.S. provisional application Ser. No. 61/409,579, filed Nov. 3, 2010, the contents of which are herein incorporated by reference in its entirety.

FIELD OF THE INVENTION

This invention relates to the field of integrated circuits. More particularly, this invention relates to polysilicon resistors in CMOS integrated circuits.

BACKGROUND OF THE INVENTION

Modern integrated process flows typically may have many patterning and implantation steps to form the variety of transistors in an IC. For example, core transistors with low turn on voltage (vt), nominal vt, and high vt may be formed in addition to input/output (I/O) transistors and memory cell transistors such as SRAM transistors. Each transistor type typically requires a vt pattern and implant, gate doping pattern and implant, a source and drain extension pattern and implant, and a deep source and drain pattern and implant. A CMOS process flow typically builds both a pmos and nmos transistor of each transistor type. A CMOS flow with 3 core transistor types plus SRAM transistors and I/O transistors may have 20 or more patterning and implant steps to form 5 different nmos transistors and 5 different pmos transistors. In addition if other embedded devices, such as resistors, capacitors or bipolar transistors are constructed, additional patterns and implant steps may be added.

Electronic digital and analog integrated circuits often require resistors to perform the desired functions. One type of resistor which may be formed on an integrated circuit is a polysilicon resistor. N-type or p-type polysilicon resistors are typically formed using source/drain ion implantation or gate doping ion implantation.

One important property of embedded resistors, especially for analog circuits, is the temperature coefficient of resistance (TCR) which measures the change in resistance with a change in temperature. To reach sufficiently low TCR, the impurity of doping concentration must be very high, about $3\times10^{20}/cm^3$ for polysilicon resistors. Typically, additional implants are performed in an integrated process flow with embedded polysilicon resistors to provide resistors with low TCR. These additional implants usually require one or more additional photomask levels and add cost and cycle time to the integrated circuit process flow.

SUMMARY OF THE INVENTION

The following presents a simplified summary in order to provide a basic understanding of one or more aspects of the invention. This summary is not an extensive overview of the invention, and is neither intended to identify key or critical elements of the invention, nor to delineate the scope thereof. Rather, the primary purpose of the summary is to present some concepts of the invention in a simplified form as a prelude to a more detailed description that is presented later.

A method for adding a low TCR resistor to a baseline CMOS manufacturing flow. A method of forming a low TCR resistor in a CMOS manufacturing flow. A method of forming an n-type and p-type transistor with a low TCR resistor in a CMOS manufacturing flow.

DESCRIPTION OF THE VIEWS OF THE DRAWING

FIG. **1** is a graph of the temperature coefficient of a resistor versus n-type doping density according to an embodiment.

FIG. **2** is an electrical diagram, in schematic form, illustrating a computer system for modifying a baseline CMOS process flow to add a low TCR resistor according to principles of this invention.

FIG. **3** is a flow diagram illustrating the operation of the computer system for modifying a baseline CMOS manufacturing flow to add a low TCR resistor according to principles of this invention.

FIG. **4**A through FIG. **4**J are cross sections of an integrated circuit containing a CMOS circuit and a low TCR gate material resistor, referred to hereinafter as the resistor, formed according to an embodiment, depicted in successive stages of fabrication.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

The present invention is described with reference to the attached figures, wherein like reference numerals are used throughout the figures to designate similar or equivalent elements. The figures are not drawn to scale and they are provided merely to illustrate the invention. Several aspects of the invention are described below with reference to example applications for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide an understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details or with other methods. In other instances, well-known structures or operations are not shown in detail to avoid obscuring the invention. The present invention is not limited by the illustrated ordering of acts or events, as some acts may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a methodology in accordance with the present invention.

An integrated circuit containing CMOS circuits which include polysilicon gate NMOS transistors and polysilicon gate PMOS transistors to form logic gates may also contain a polysilicon gate material resistor with a low temperature coefficient (TCR) formed by ion implanting the body region of the resistor concurrently using implants already in a baseline CMOS process flow. Implants used to form the NMOS and PMOS transistors in the CMOS logic circuits, such as the pre gate etch poly doping implants, LDD implants, and source and drain implants may concurrently implant the resistor body region. A silicide block layer is formed over the resistor body region prior to forming metal silicide on source and drain regions of the NMOS and PMOS transistors. The silicide block layer may be formed separately from the sidewall spacers on the NMOS and PMOS gates. Head regions of the resistor are ion implanted concurrently with a combination of the implants used to form the NMOS and PMOS transistors in the CMOS logic circuits, so that the head regions are the same conductivity type as the body region. In example embodiments, no additional photoresist patterns are added to the baseline